Amendments to the Drawings:

Please replace original figures 1-5, and 7-9 with replacement figures 1-5, and 7-9, respectively.

Attachment: Replacement Sheets 8 page(s)

REMARKS

Figures 1-9 are objected to under 37 CFR 1.84o because all features represented by boxes in the figures must be labeled with a term which indicates what element the boxes represent.

Applicant has included replacement sheets for Figures 1-5, and 7-9. The following describes the changes made the drawings. No new matter is entered.

Fig.1: The term D-Flip flop is added to label element 102, and the term Scan cell is added to label element 100.

Fig.2: The term D-Flip flop scan cell is added to elements 210 and 230.

Fig.3: The term D-Flip flop scan cell is added to label elements 512, 514, 516, 522, 520, and 532.

Fig.4: The term D-Flip flop scan cell is added to label elements 512, 514, 516, 522, 520, and 532; and the term Clock domain is added to label elements 510, 520, and 530.

Fig.5: The term D-Flip flop scan cell is added to label elements 512, 514, 516, 522, 520, and 532; and the term D-Latch is added to label element 704.

Fig.7: The term D-Flip flop scan cell is added to label elements 914, 916, 918, 924, 926, and 934.

Fig.8: The term D-Flip flop and the term Scan cell is added to label element 924.

Fig.9: The term D-Flip flop scan cell is added to label elements 914, 916, 918, 924, 926, and 934.

Claims 1 and 6 are rejected because of the informality the term "the clock tree quasi-balance characteristic" lacks antecedent basis. It is also not clear what actually is a clock tree-quasi-balance characteristic. Claim 2-5 and 7 are objected because they depend on claims 1 and 6 and contain the same problem of indefiniteness.

Applicant has amended claim 1 to delete the term "the clock tree quasi-balance characteristic" from claim 1. However, the applicant does not agree with the Examiner's view as to the unclearness of the meaning, or definition, of the term "clock tree quasi-balance characteristic", and similarly, the term "clock tree balance characteristic", both of which are currently incorporated in amended claims 6 and 13. The applicant would like to point out to the Examiner that the meaning or definition of the terms "clock tree quasi-balance characteristic" and "clock tree quasi-balance characteristic" are well laid out in paragraph [0025], page 7 of the patent application document as originally filed, and this should leave no ambiguity as to the meaning of such terms.

Claims 8-9 are rejected under 35 USC 103a as being unpatentable over Peeters et al. (6,393,592 and Peeters hereinafter).

Applicant has cancelled claims 8-9.

New Claims 10-15

Applicant has added new claims 10-15. No new matter is introduced by the newly added claims. Concerning the patentability of new independent claim 10 with respect to the teachings of Peeters et al., applicant points out that Peeters et al. do not teach at least the following steps as claimed in claim 10:

operating the first clock domain referencing to a first clock signal during the first mode;

operating the second clock domain referencing to a second clock signal being of a frequency different from a frequency of the first clock signal during the first mode;

operating the first clock domain referencing to the first clock signal to perform a scan test in the first clock domain during the second mode; and

operating the second clock domain referencing to the first clock signal to perform the scan test in the second clock domain during the second mode.

Peeters et al. teach in col 4, lines 29-33 that "it is possible to route two separate clocks to the scan-flop 200. Preferably, one clock is a regular functional system clock, and the other clock is a dedicated scan clock." Peeters et al. also state in col 4, lines 59-62 that "this design therefore provides a simple and compact integrated design that will eliminate the problems associated with multiple clock domains and the difficulty of skew management." However, Peeters et al. do not teach a design having two clock domains where the first and second clock domains are operated using different clocks during a first mode, but are operated using a same clock during a second mode. This should not be found obvious given the teachings of Peeters because no suggestion is made that different clock domains should actually use the same clock during a particular mode. This is in contrast to the definition of different clock domains assumed by Peeters. That is, that different clock domains use different clock signals. For at least this reason applicant asserts that new independent claim 10 should be found allowable with respect to the teachings of Peeters et al. If claim 10 is found allowable, so too should the dependent claims 11-15. Consideration of new claims 10 to 15 is respectfully requested.

Sincerely yours,

Winston Hsu Date: 12/13/2005

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)